

Fig. 1

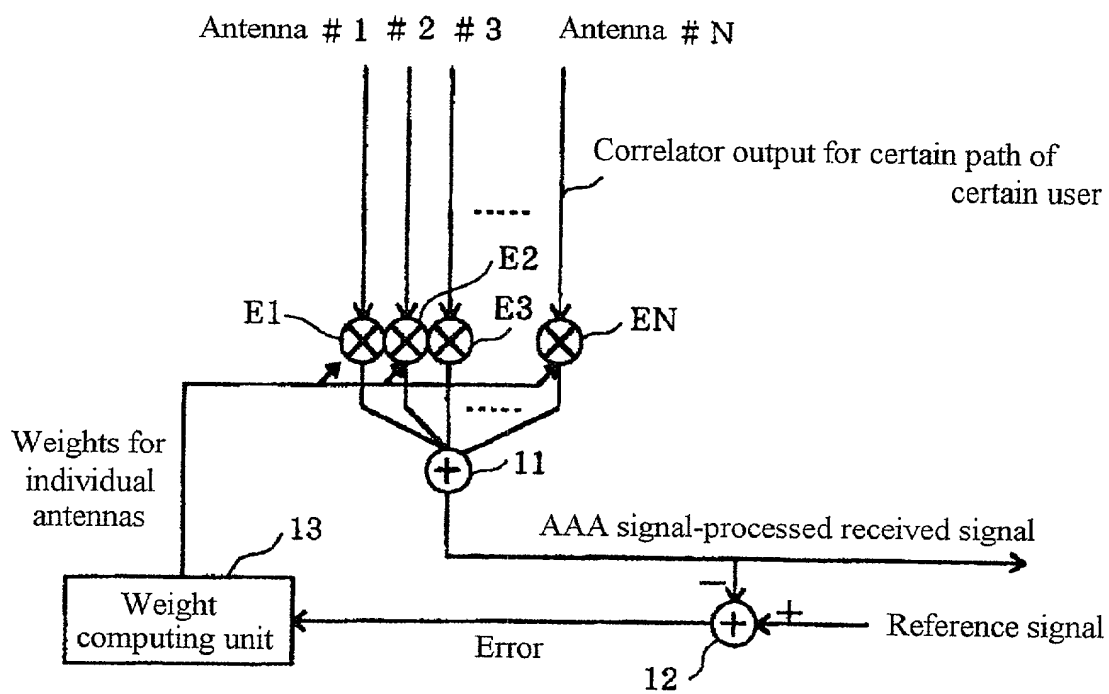


Fig. 2

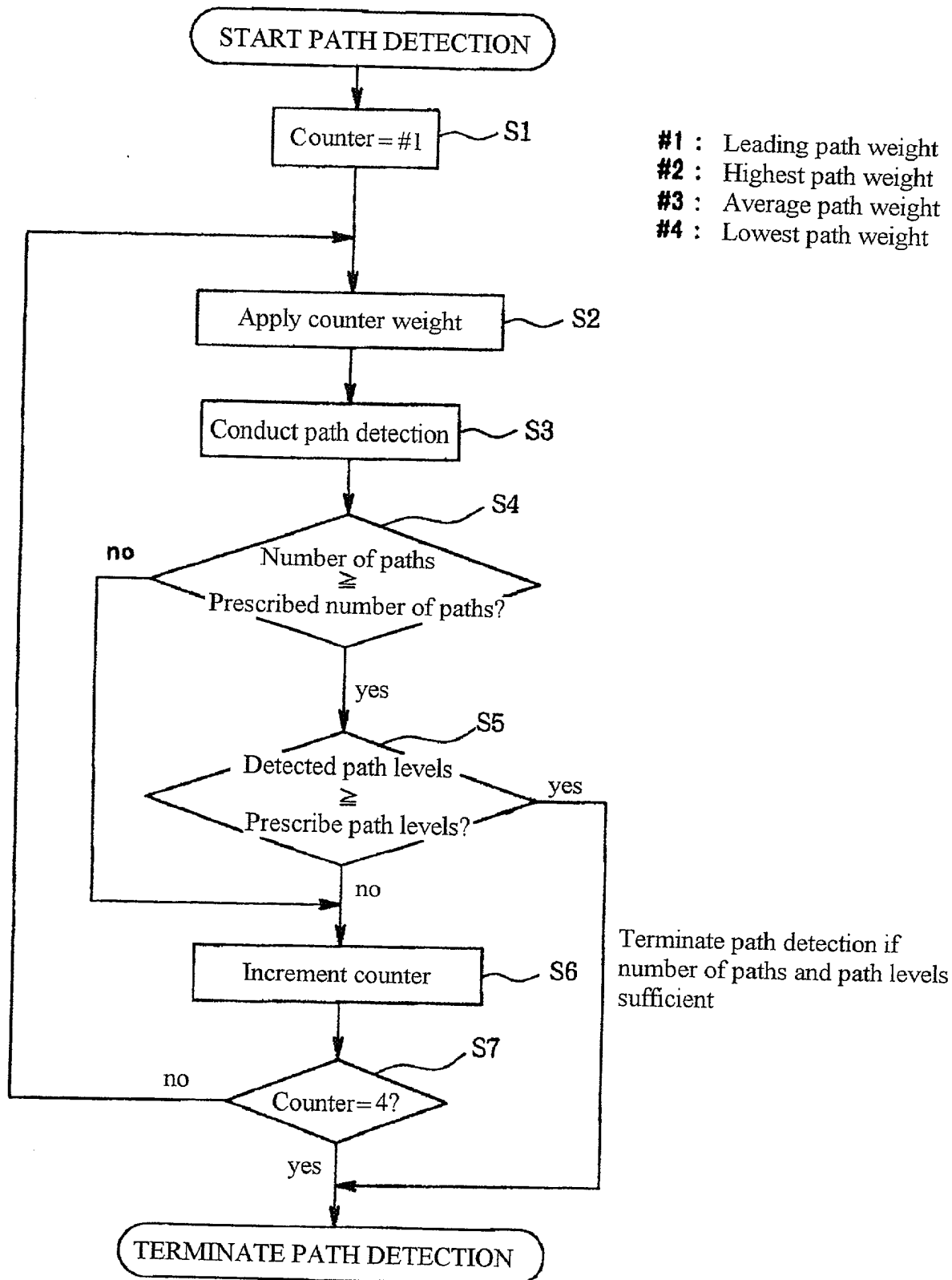
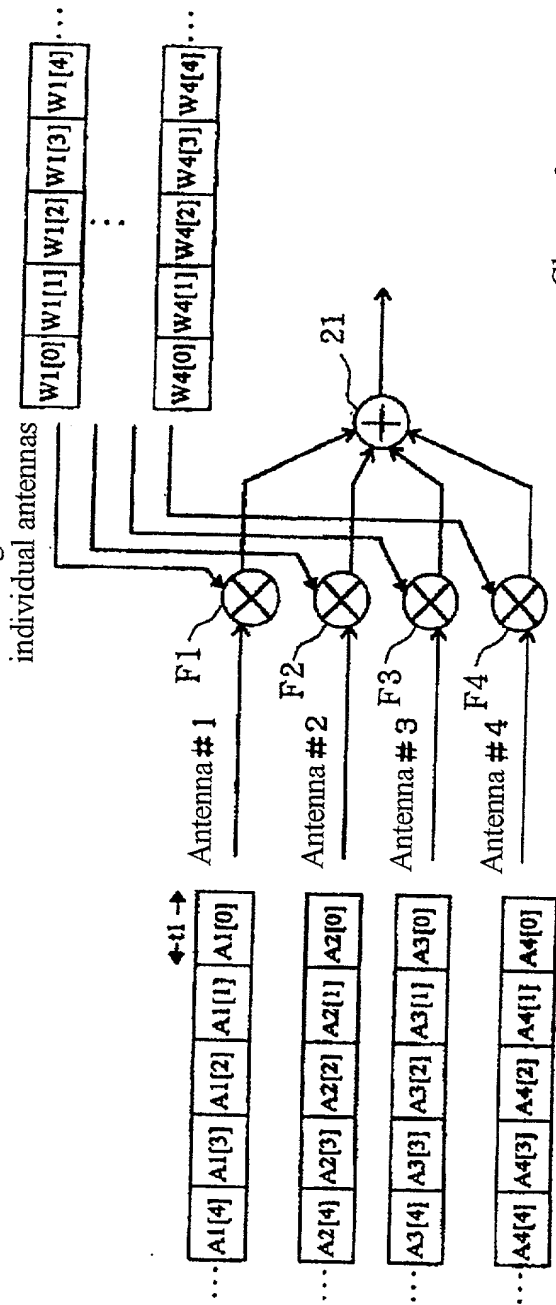
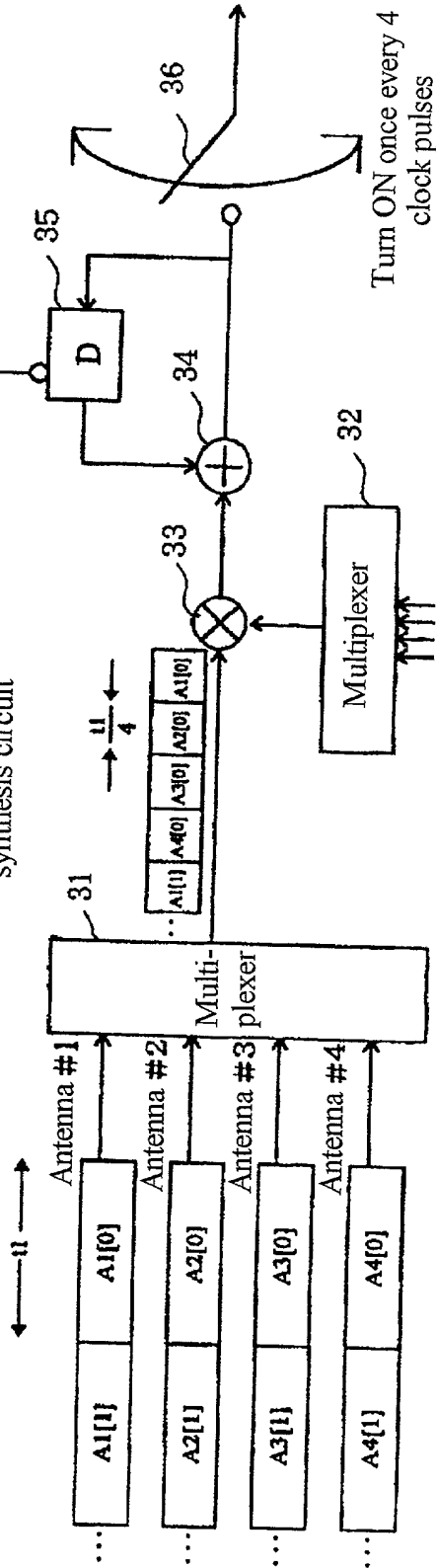


Fig. 3



(a) Ordinary weight multiplication & synthesis circuit



(b) Weight multiplication & synthesis circuit using time division

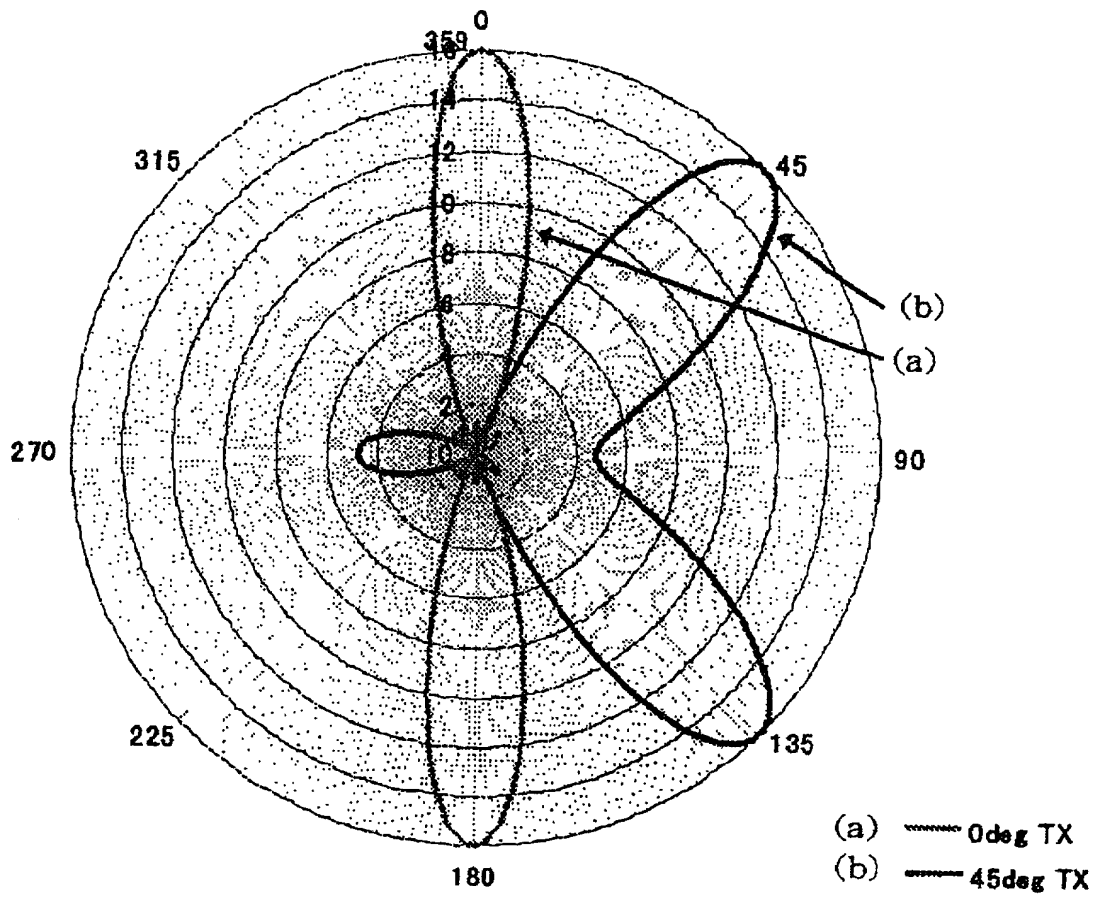


Fig. 5

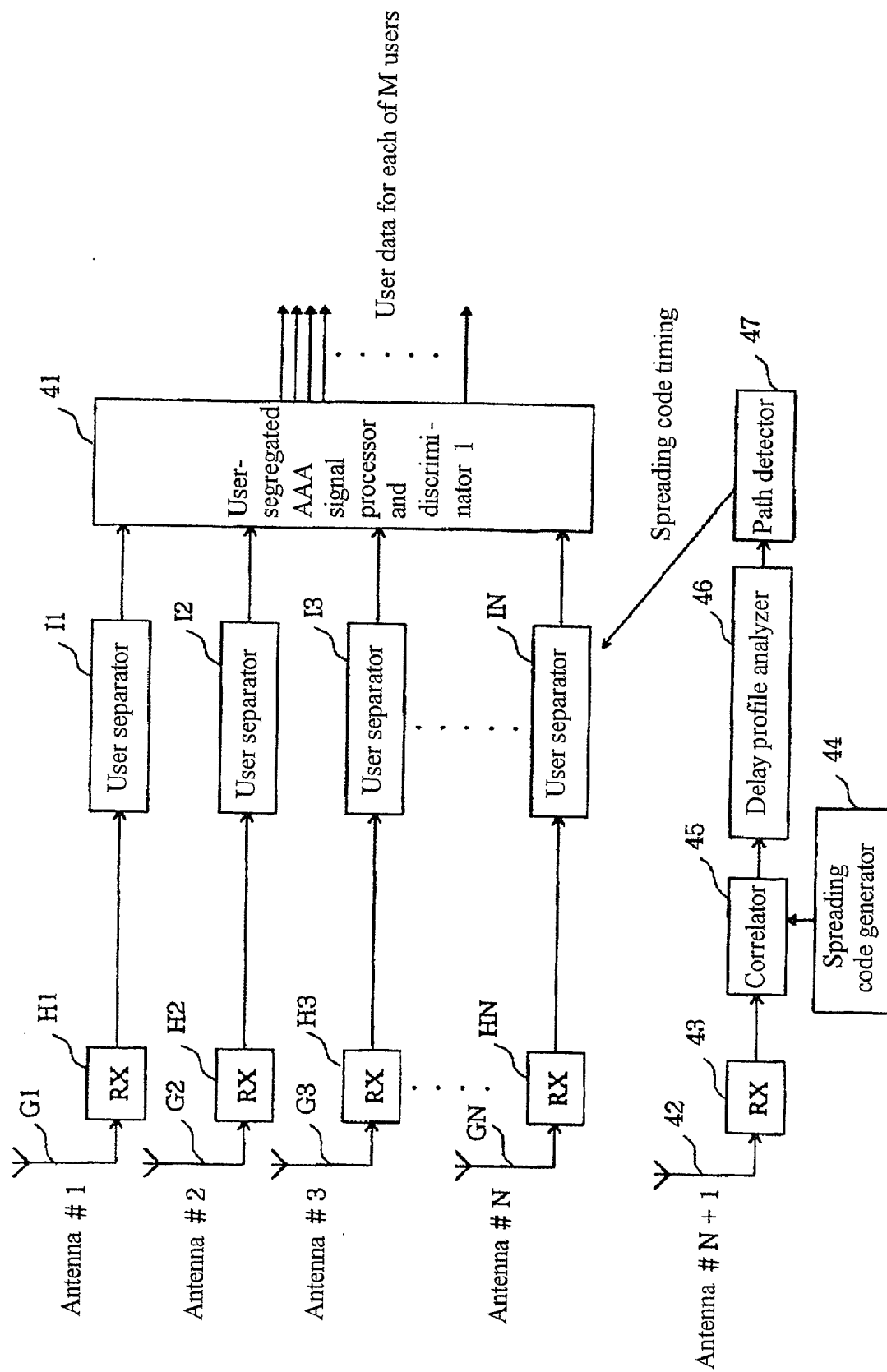


Fig. 6

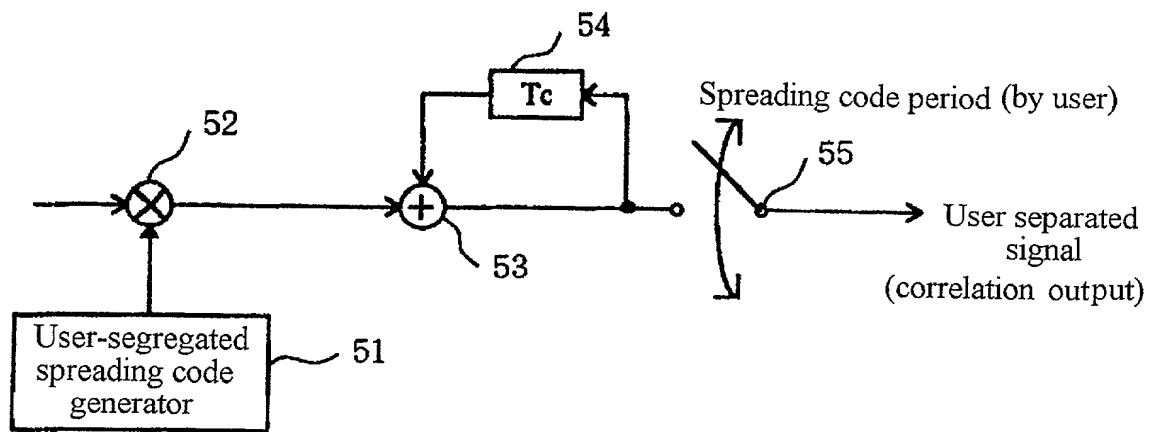


Fig. 7

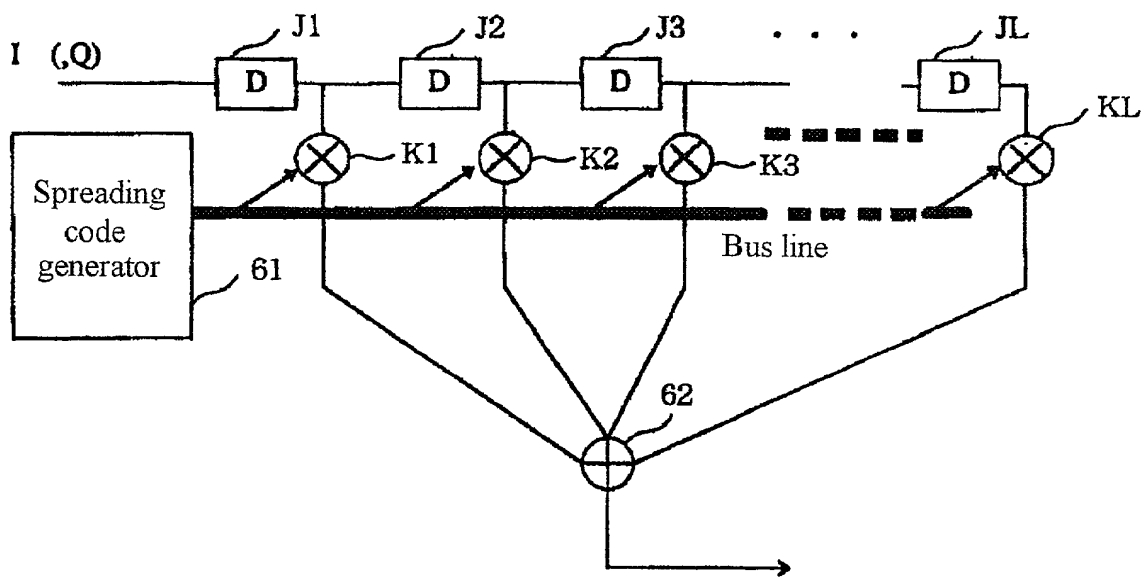


Fig. 8

0995982-092001
100250-28655660

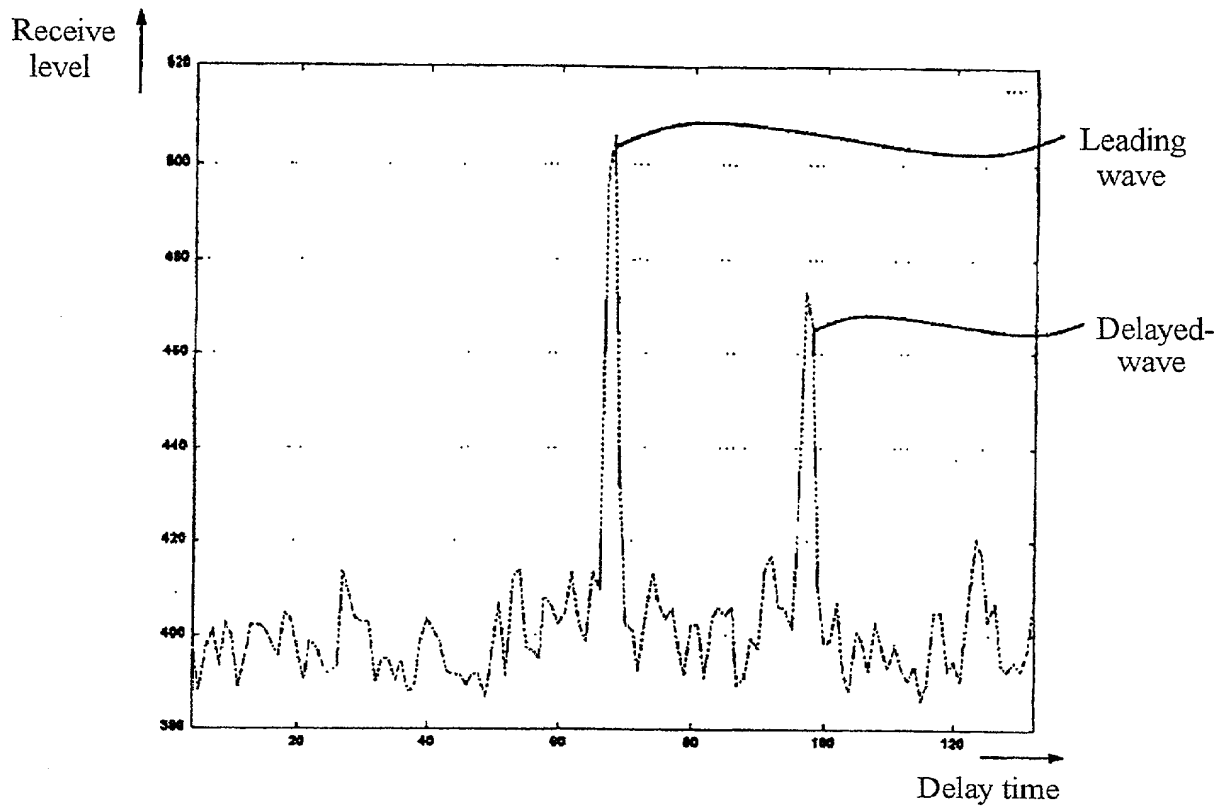


Fig. 9

100

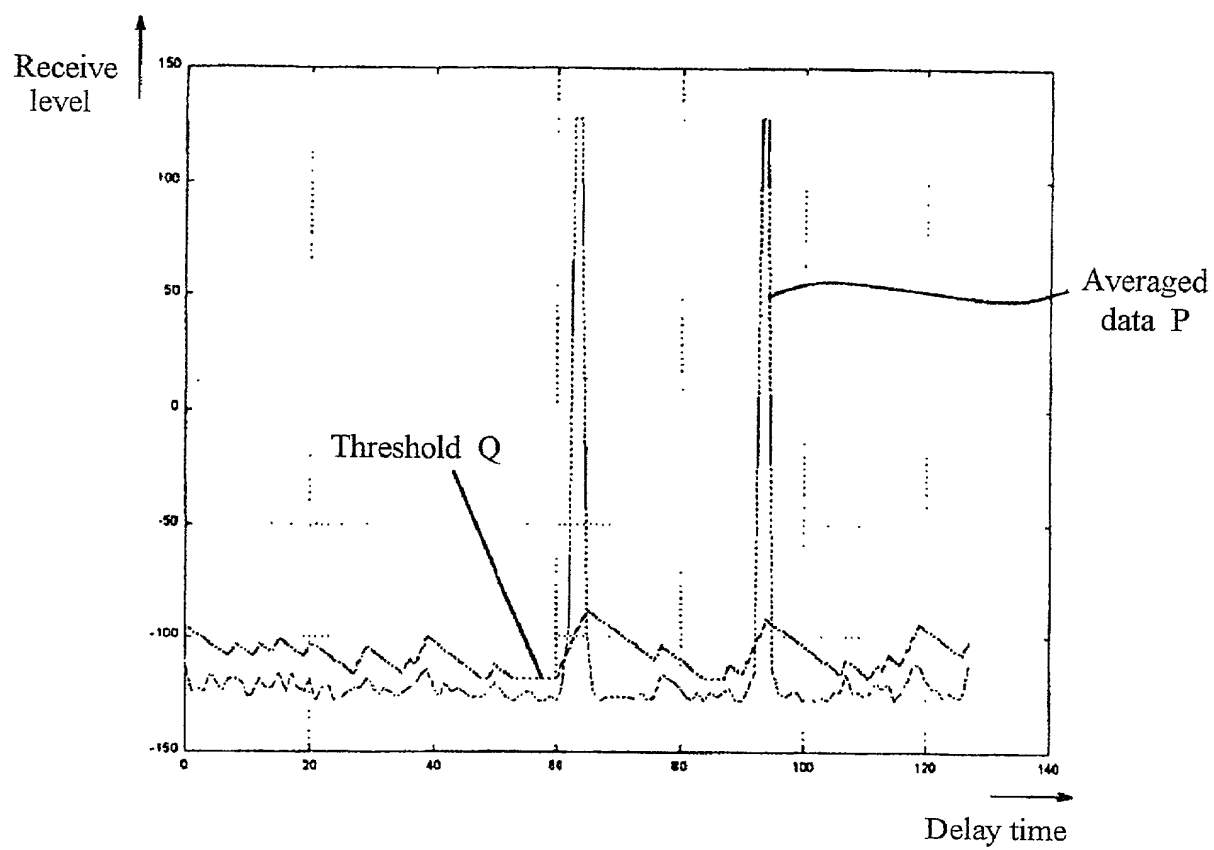


Fig. 10